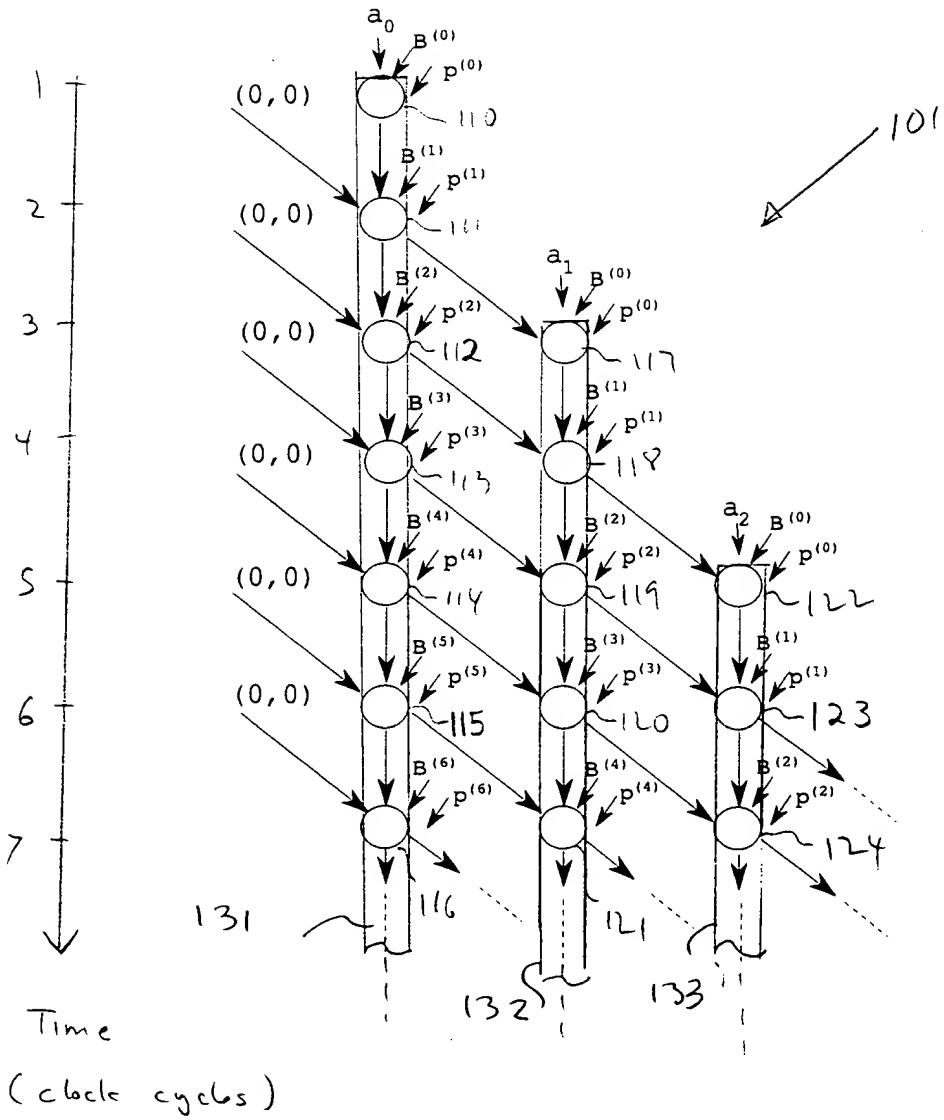
101
a_0
$B^{(0)}$
$p^{(0)}$
110
(0,0)
$B^{(1)}$
$p^{(1)}$
111
(0,0)
$B^{(2)}$
$p^{(2)}$
112
(0,0)
$B^{(3)}$
$p^{(3)}$
113
(0,0)
$B^{(4)}$
$p^{(4)}$
114
(0,0)
$B^{(5)}$
$p^{(5)}$
115
(0,0)
$B^{(6)}$
$p^{(6)}$
116
a_1
$B^{(0)}$
$p^{(0)}$
117
$B^{(1)}$
$p^{(1)}$
118
$B^{(2)}$
$p^{(2)}$
119
$B^{(3)}$
$p^{(3)}$
120
$B^{(4)}$
$p^{(4)}$
121
a_2
$B^{(0)}$
$p^{(0)}$
122
$B^{(1)}$
$p^{(1)}$
123
$B^{(2)}$
$p^{(2)}$
124
131
132
133
1
2
3
4
5
6
7
Time
(clock cycles)

FIG. 1

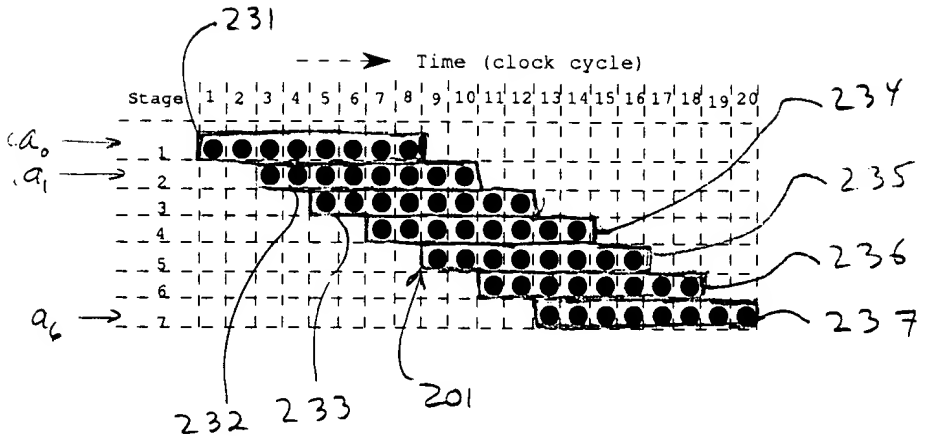
231
Time (clock cycle)
Stage
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
a_0
a_1
a_6
1
2
3
4
5
6
7
234
235
236
237
232
233
201

FIG. 2

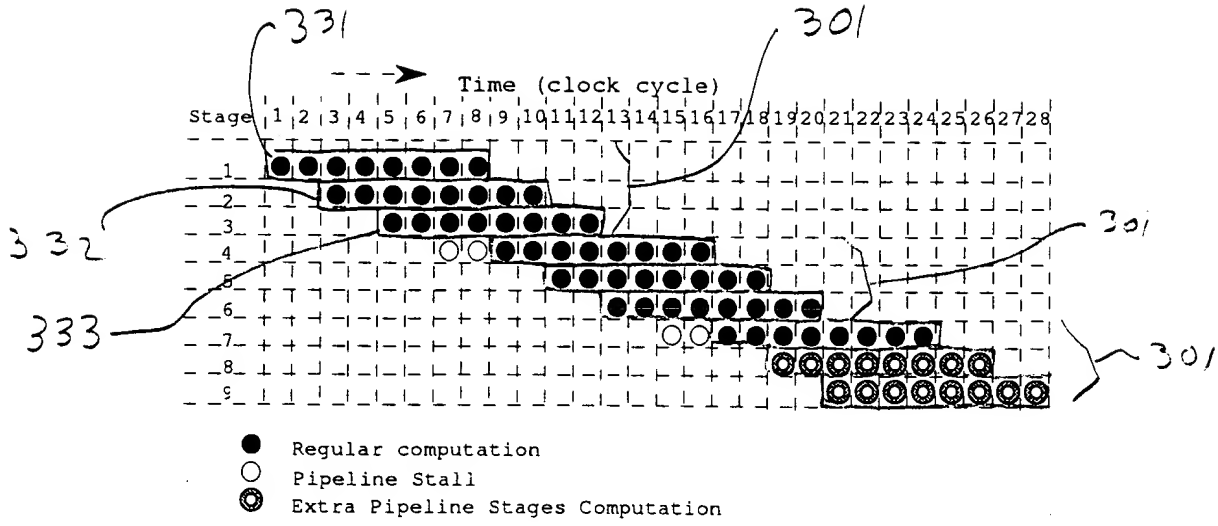
331
301
Time (clock cycle)
Stage 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28
1
2
3
4
5
6
7
8
9
332
333
301
301
Regular computation
Pipeline Stall
Extra Pipeline Stages Computation

FIG. 3

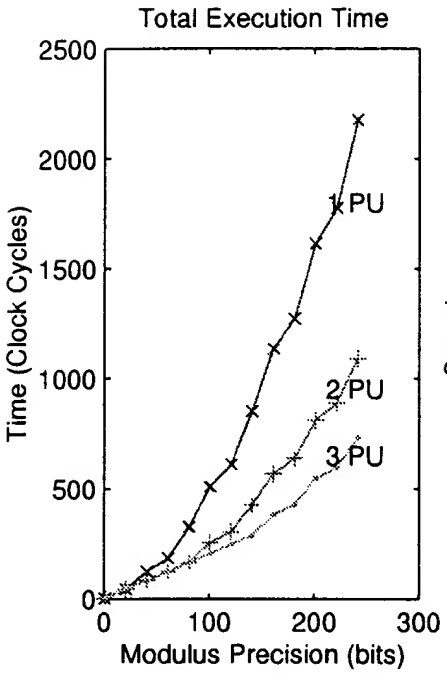

FIG. 4A

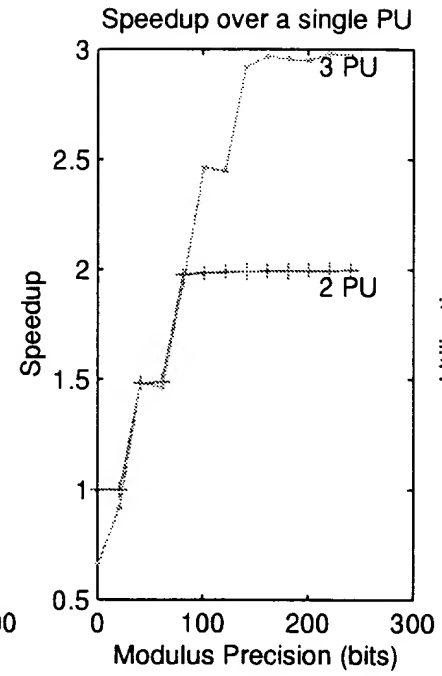

FIG. 4B

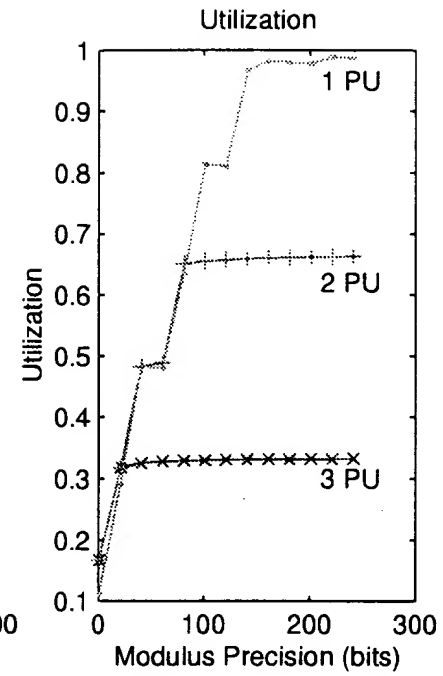

FIG. 4C

FIG. 4

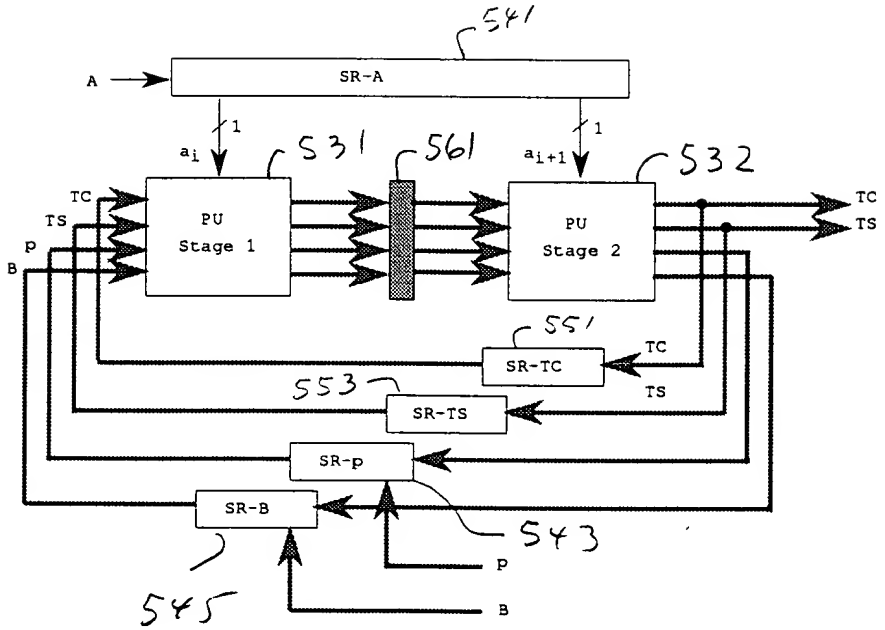
541
A
SR-A
a_i
1
531
561
a_{i+1}
1
532
TC
TS
p
B
PU
Stage 1
PU
Stage 2
TC
TS
551
SR-TC
TC
TS
553
SR-TS
SR-p
SR-B
543
p
B
545

FIG. 5

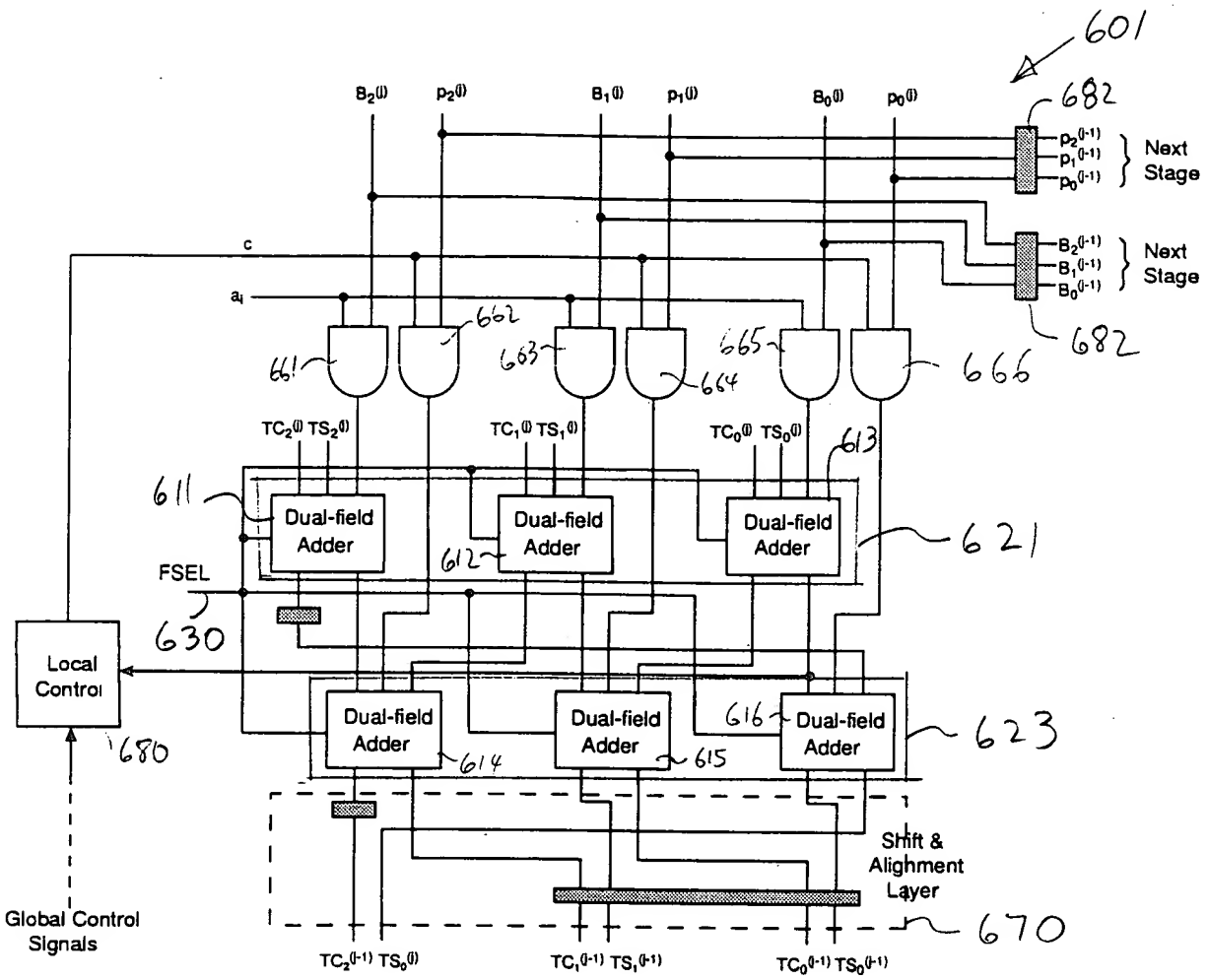
601
682
Next Stage
Next Stage
682
c
a_i
661
662
663
664
665
666
611
612
613
621
623
FSEL
630
Local Control
680
Dual-field Adder
614
615
616
Shift & Alighment Layer
670
Global Control Signals

FIG. 6

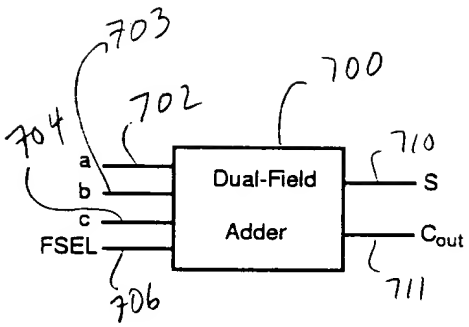

FIG. 7A

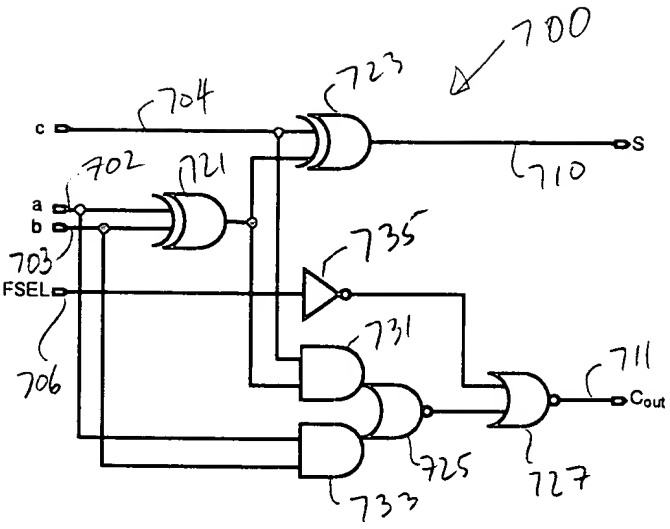

FIG. 7B

FIGS. 7A-7B

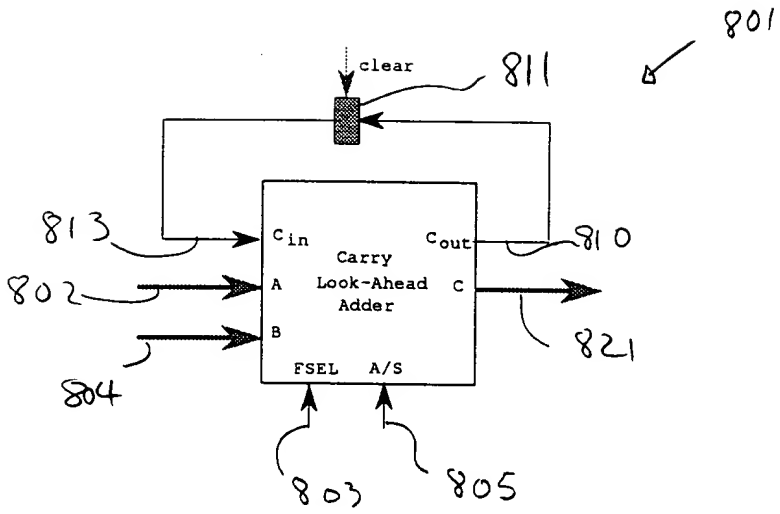
801
clear
811
813
Cin
Cout
Carry
Look-Ahead
Adder
810
802
A
C
B
821
804
FSEL
A/S
803
805

FIG. 8

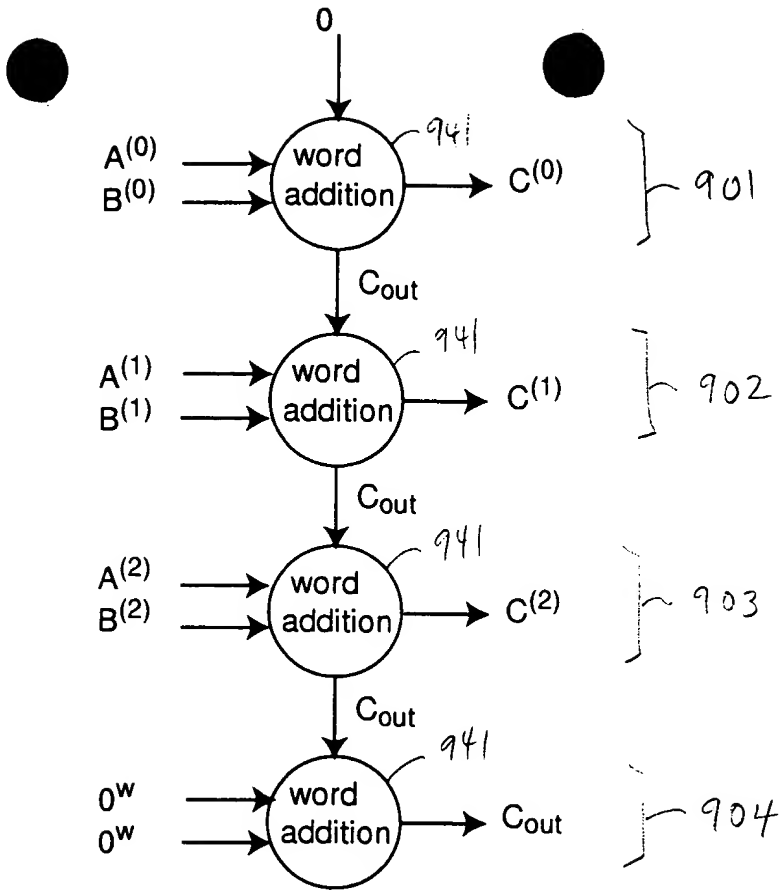

FIG. 9

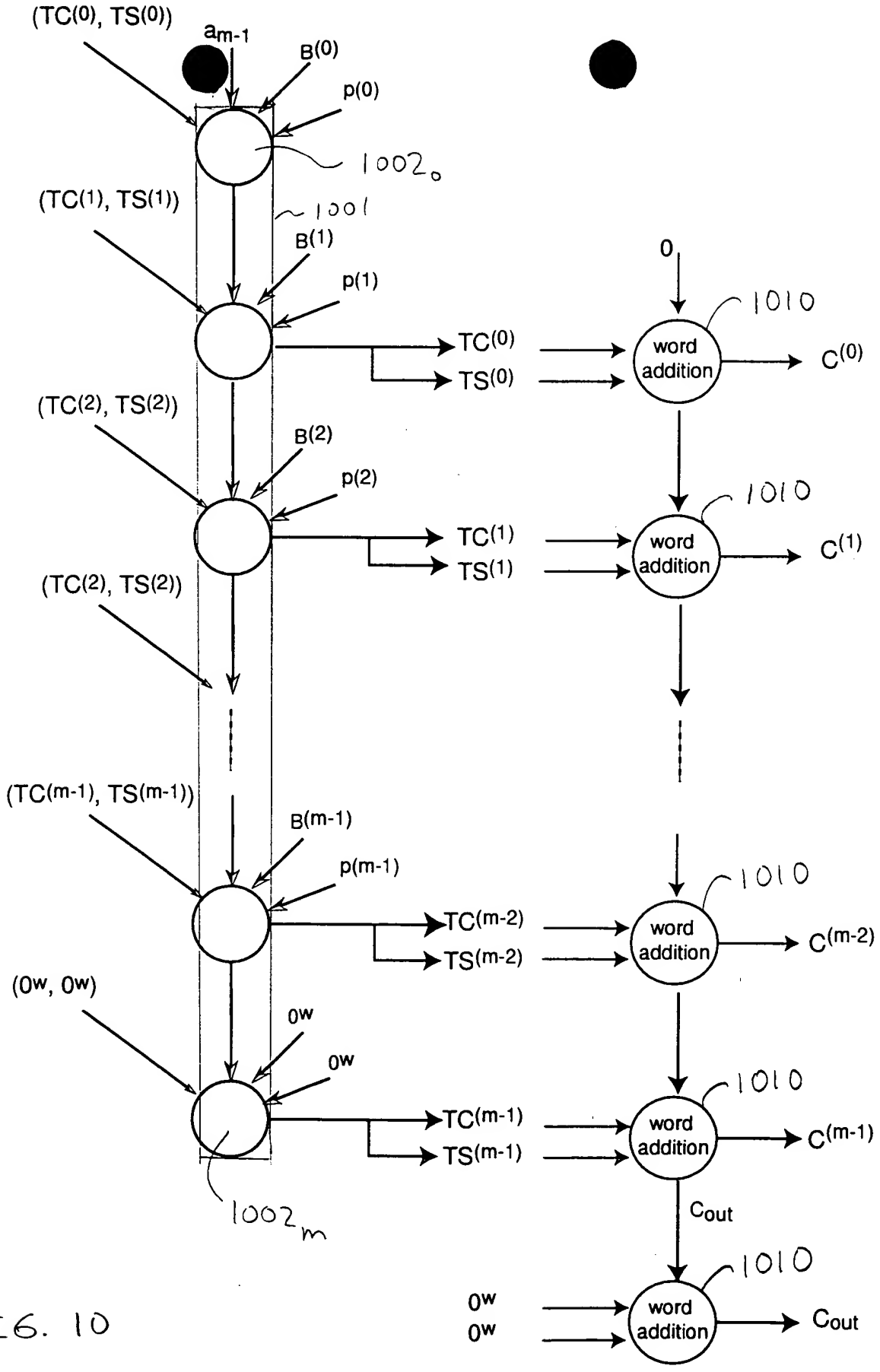
(TC(0), TS(0))
a_{m-1}
B(0)
p(0)
1002₀
1001
(TC(1), TS(1))
B(1)
p(1)
TC(0)
TS(0)
0
1010
word addition
C(0)
(TC(2), TS(2))
B(2)
p(2)
TC(1)
TS(1)
1010
word addition
C(1)
(TC(2), TS(2))
(TC(m-1), TS(m-1))
B(m-1)
p(m-1)
TC(m-2)
TS(m-2)
1010
word addition
C(m-2)
(0w, 0w)
0w
0w
TC(m-1)
TS(m-1)
1010
word addition
C(m-1)
1002m
Cout
1010
0w
0w
word addition
Cout

FIG. 10

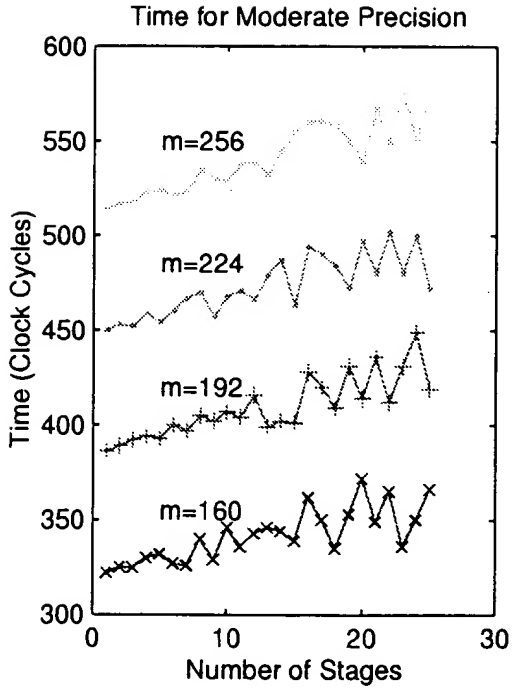

FIG. 11A

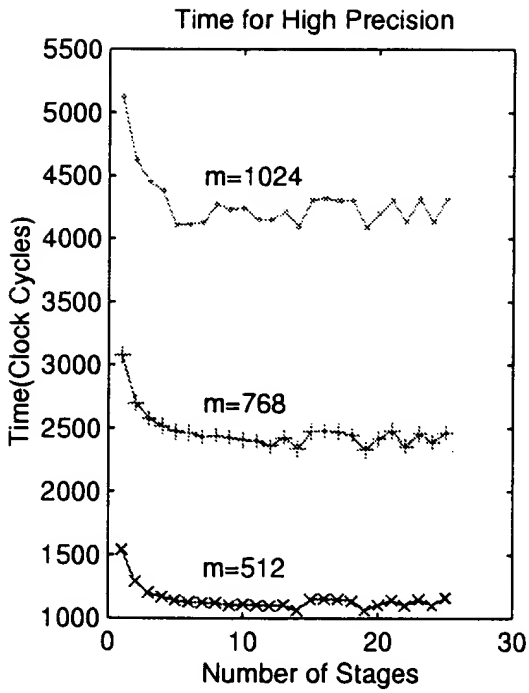

FIG. 11B

FIG. 11